



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/620,040	07/15/2003	Michael I. Thompson	QN1022.US	7524
22145 7590 09/04/2007 KLEIN, O'NEILL & SINGH, LLP 43 CORPORATE PARK SUITE 204 IRVINE, CA 92606			EXAMINER MUI, GARY	
			ART UNIT 2616	PAPER NUMBER
			MAIL DATE 09/04/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/620,040

Applicant(s)

THOMPSON, MICHAEL I.

Examiner

Gary Mui

Art Unit

2616

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 June 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 5-7, 9-22 and 24-26 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 5-7, 9-22 and 24-26 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 15 June 2007 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 5 – 7, 9 – 22, and 24 – 26 have been considered but are moot in view of the new ground(s) of rejection.
2. Claims 1 – 4, 8, 23, 27, and 28 has been cancelled as indicated by the amendment dated June 15, 2007.
3. Claims 5 – 7, 9 – 22 and 24 – 26 are now currently pending.

Drawings

4. The drawings were received on June 15, 2007. These drawings are acceptable.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Art Unit: 2616

7. Claims 5 – 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (US 6,526,446 B1, hereinafter “Yang”) in view of Savarda et al. (US 2003/0196081 A1; hereinafter Savarda).

For claim 5, Yang teaches an inbound MAC receive state machine for processing MAC frames received from a network (see column 2 lines 35 – 37); an inbound IP verifier state machine for verifying IP packet headers (see column 9 lines 21 – 32); an inbound IP fragment processing state machine for processing and reassembling IP fragments (see column 9 lines 11 – 20); and an inbound TCP state machine for processing TCP segments received from an IP layer (see column 6 lines 51 – 55). Yang fails to teach the inbound IP verifier state machine passes non-IP data packets to a host. Savarda from the same field of endeavor teaches the packet-object may be passes thought the packet co-processor as a non-IP packet without any IP processing (see paragraph 0029). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to pass non-IP packets as taught by Savarda into network interface card taught by Yang. The motivation for doing this is to increase the speed of the system where unnecessary IP processing is avoided.

For claim 6, Yang teaches the inbound IP verifier state machine verifies IP packet header information and if the header information is valid, then temporary stores the packet in an external memory (see column 9 lines 21 – 41; after checksum IP packet is placed on Tx FIFO memory).

For claim 7, Yang teaches all of the claimed subject matter with the exception of the inbound IP verifier state machine passes complete IP datagrams to the host that are non-TCP packets. Savarda from the same field of endeavor teaches the packet-object may be passes thought the

Art Unit: 2616

packet co-processor as a non-IP packet without any IP processing (see paragraph 0029). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to pass non-IP packets as taught by Savarda into the network interface card taught by Yang. The motivation for doing this is to increase the speed of the system where unnecessary IP processing is avoided.

Claim Rejections - 35 USC § 103

8. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang in view of Trippe (US 2003/0108066 A1).

For claim 9, Yang teaches an inbound MAC receive state machine for processing MAC frames received from a network (see column 2 lines 35 – 37); an inbound IP verifier state machine for verifying IP packet headers (see column 9 lines 21 – 32); an inbound IP fragment processing state machine for processing and reassembling IP fragments (see column 9 lines 11 – 20); and an inbound TCP state machine for processing TCP segments received from an IP layer (see column 6 lines 51 – 55). Yang fails to teach the inbound TCP state machine maintains a segment re-assembly list for each network connection that is linked to a network control block and is used to re-order out of order TCP data segments. Trippe from the same field of endeavor teaches storing in a content-addressable memory about the packet received like the sequence identifier for reordering the packet (see paragraph 0004 and 0005). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to maintain a reassembly list as taught by Tripp into the network interface

card as taught by Yang. The motivation for doing this is to increase the efficiency of the system where in an order list is maintained prior to reassembly of a packet.

For claim 10, Yang teaches the inbound TCP state machine passes in-order TCP segments to the host or to an upper layer protocol processor (see column 9 lines 3 – 20).

Claim Rejections - 35 USC § 103

9. Claims 11 – 14, 16, 18, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang in view of Hayes (US 2003/0046330 A1).

For claim 11, Yang teaches a verification module that verifies incoming data packets (see column 9 lines 21 – 32); a first in-bound TCP processor for processing TCP segments received from a network (see column 6 lines 51 – 55); a fragment processor that receives data packet fragments and reassembles the data packet fragments into complete datagrams for delivery (see column 9 lines 11 – 20). Yang fails to teach a second in-bound processor for processing incoming TCP segments destined for iSCSI. Hayes from the same field of endeavor teaches the use of an auxiliary processor the can process TCP segments for iSCSI (see paragraph 0017). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to have a second processor as taught by Hayes into the network interface card of Yang. The motivation for doing this is to increase the efficiency of the system by separating processes.

For claim 12, Yang teaches a first outbound processor that processes TCP data that is sent to the network (see column 10 lines 7 – 10); and a second outbound processor that processes MAC and IP transfers to the network machine (see column 9 lines 51 – 55).

For claim 13, Yang teaches the second outbound processor also acts as a pass through processor for TCP data processed by the first outbound processor (see column 10 lines 7 – 10).

For claim 14, Yang teaches the first outbound processor builds TCP header data and passes the header data to the second outbound processor (column 7 lines 44 – 65).

For claim 16, Yang teaches the verification module verifies IP data packet header information and if the header information is valid, then the data packet is added to a list maintained by the verification module (see column 9 lines 21 – 41).

For claim 18, Yang teaches the fragment processor sets a flag if overlapping datagrams are received, and the flag indicates when a TCP checksum must be re-run (see column 6 line 51 – column 7 line 15 and column 9 line 21 – 35).

For claim 22, Yang teaches the first inbound processor receives a data segment with a TCP header and option data (see 6 lines 51 – 67).

Claim Rejections - 35 USC § 103

10. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yang and Hayes as applied to claim 11 above, and further in view of Savarda.

For claim 15, Yang teaches all of the claimed subject matter with the exception of the verification module passes non-IP data packets to a host. Savarda from the same field of endeavor teaches the packet-object may be passes thought the packet co-processor as a non-IP packet without any IP processing (see paragraph 0029). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to pass non-IP

Art Unit: 2616

packets as taught by Savarda into network interface card taught by Yang. The motivation for doing this is to increase the speed of the system where unnecessary IP processing is avoided.

Claim Rejections - 35 USC § 103

11. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yang and Hayes as applied to claim 11 above, and further in view of Chang et al. (US 7,103,317 B2, hereinafter "Chang").

For claim 17, Yang and Hayes teaches all of the claimed subject matter with the exception of the fragment processor provides a timer to time each datagram reassembly with a programmable default timer value. Chang from the same field of endeavor teaches the use of a reassembly timer when it receives an initial fragment (see column 8 lines 45 – 51). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use a timer as taught by Chang into the network interface card of Yang. The motivation for doing this is to provide an efficient system.

Claim Rejections - 35 USC § 103

12. Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang and Hayes as applied to claim 11 above, and further in view of Trippe.

For claim 19, Yang and Hayes teaches all of the claimed subject matter with the exception of the first inbound processor re-orders out of order data segment. Trippe from the same field of endeavor teaches with the use of content-addressable memory it enables the system to order the packets into their proper sequence thought the packets may have arrived out of order (see

Art Unit: 2616

paragraph 0013). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to reorder out of order data segments as taught by Trippe into the network interface card of Yang. The motivation for doing this is to increase the efficiency of system.

For claim 20, Yang and Hayes teaches all of the claimed subject matter with the exception of the first inbound processor maintains a segment re-assembly list for each network connection that is linked to a network control block. Trippe from the same field of endeavor teaches storing in a content-addressable memory about the packet received like the sequence identifier for reordering the packet (see paragraph 0004 and 0005). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to maintain a reassembly list as taught by Tripp into the network interface card as taught by Yang. The motivation for doing this is to increase the efficiency of the system where in an order list is maintained prior to reassembly of a packet.

Claim Rejections - 35 USC § 103

13. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yang and Hayes as applied to claim 21 above, and further in view of Boucher et al. (US 6,247,060 B1, hereinafter "Boucher").

For claim 21, Yang teaches the first inbound processor includes a receive block that receives data (see column 2 lines 22 – 37), a validation block that validates data segments (see column 9 lines 21 – 24). Yang fails to teach an option block for validating a TCP timestamp that is found in TCP option data; and acknowledgement processor that performs TCP

Art Unit: 2616

acknowledgement processing. Boucher from the same field of endeavor teaches header validation where the timestamp option is validated if present and an ACK will be set (see column 58 lines 41 – 61). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to validate a timestamp as taught by Boucher into the network interface card of Yang. The motivation for doing this is to increase the reliability of the system.

Claim Rejections - 35 USC § 103

14. Claims 24 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang in view of Boucher.

For claim 24, Yang teaches an input processing module that determines if a TCP connection is established and checks for TCP flags to determine if a TCP data packet should be processed (see column 11 lines 23 – 29; enablement flags). Yang fails to teach an acknowledgement processor module that handles any acknowledgement information included in the TCP packet; and a Data processor module that handles any data included in the TCP data packet; wherein the first input processing module validates and saves TCP timestamps by checking if a received timestamp is greater than a most recently saved timestamp. Boucher from the same field of endeavor teaches validating the content and the timestamp values and sending back acknowledgments once validated (see column 2 lines 47 – 63 and column 58 lines 41 – 61). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to validate the packet as taught by Boucher into the network interface card of Yang. The motivation for doing this is to increase the reliability of the system.

Art Unit: 2616

For claim 26, Yang teaches the TCP connection state is organized in network control blocks and stored in a local memory (see column 7 lines 16 – 43).

Claim Rejections - 35 USC § 103

15. Claim 25 rejected under 35 U.S.C. 103(a) as being unpatentable over Yang and Boucher as applied to claim 24 above, and further in view of Trippe.

For claim 25, Yang and Boucher teaches all of the claimed subject matter with the exception of the Data Processor module determines if a received packet was in order or out of order and trims the packet if it requires trimming. Trippe teaches the use of a content-addressable memory that reads the packet sequence number to see if it is out of order and will reorder it (see paragraphs 0012 and 0013). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to maintain a find out of order packet by Tripp into the network interface card as taught by Yang. The motivation for doing this is to increase the efficiency of the system where in an order list is maintained prior to reassembly of a packet.

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Basso et al. (US 2002/0156908 A1) and Beckwith et al. (US 2002/0174244 A1) are recited to show a method and system for processing network data packets.

Art Unit: 2616

17. **Examiner's Note:** Examiner has cited particular paragraphs or columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

In the case of amending the claimed invention, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary Mui whose telephone number is (571) 270-1420. The examiner can normally be reached on Mon. - Thurs. 9 - 3 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on (571) 272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

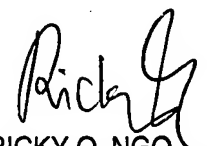
Art Unit: 2616

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



GM

02.28.2007



RICKY Q. NGO
SUPERVISORY PATENT EXAMINER